

<b>LIST OF REFERENCES CITED BY APPLICANT</b> (Use several sheets if necessary)	ATTY. DOCKET NO. 100665.0044US1	SERIAL NO. 10/026,338
	APPLICANT Jesse Pedigo	
	FILING DATE 12/20/01	GROUP 1725



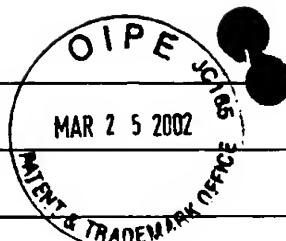
### U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
KS	5,851,344	12/22/98	Ultrasonic Wave Assisted Contact Hole Filling	156	379.6	12/22/98
	5,906,042	05/25/99	Method and Structure to Interconnect Traces of Two Conductive Layers in a Printed Circuit Board	29	852	10/04/95
	5,925,414	07/20/99	Nozzle and Method for Extruding Conductive Paste into High Aspect Ratio Openings	427	282	07/20/99
	5,994,779	11/30/99	Semiconductor Fabrication Employing a Spacer Metallization Technique	257	773	05/02/97
	6,000,129	12/14/99	Process for Manufacturing a Circuit with Filled Holes	29	852	03/12/98
	6,009,620	01/04/00	Method of Making a Printed Circuit Board Having Filled Holes	29	852	07/15/98
	6,079,100	06/27/00	Method of Making a Printed Circuit Board Having Filled Holes and Fill Member for Use Therewith	29	852	05/12/98
	6,090,474	07/18/00	Flowable Compositions and Use in Filling Vias and Plated Through-Holes	428	209	07/18/00
	6,106,891	08/22/00	Via Fill Compositions for Direct Attach of Devices and Method for Applying Same	427	97	12/18/98
	6,138,350	10/31/00	Process for Manufacturing a Circuit Board with Filled Holes	29	852	02/25/98
	6,153,508	11/28/00	Multi-Layer Circuit Having a Via Matrix Interlayer Connection and Method for Fabricating the Same	438	622	02/19/98
	6,276,055	08/21/01	Method and Apparatus for Forming Plugs in Vias of a Circuit Board Layer	29	852	09/24/98
	6,281,448	08/28/01	Printed Circuit Board and Electronic Components	174	260	08/10/99
KS	6,282,782	09/04/01	Forming Plugs in Vias of Circuit Board Layers and Subassemblies	29	852	09/02/99

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### FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
KS	EP 0 194 247 A2						



KS	EP 0 713 358 A2								
	EP 0 723 388 A1								
	GB 2 120 017 A								
	GB 2 341 347 A								
	GB 2 246 912 A								
	JP 04239193								
	JP 05275819								
	JP 53-10487								
	JP 54-139065								
	JP 62-277794								
	JP 62-287696								
	JP 03004595								
	JP 04186792								
	JP 07176871								
	JP 08172265								
	JP 08191184								
	JP 09321399								
	JP 09083135								
	JP 10065339								
	JP 10256687								
	JP 11054909								
	JP 1173696								
	JP 1236694								
	JP 58011172								
	FR 2 684 836								
	FR 2 714 567								
KS	WO 86/06243								

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OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)



KS.	Via Etching Process, February 1972
KS	Multilayer Printed Circuit Board Connections, April 1996
KS	Process for Forming Copper Clad Vias, August 1989
EXAMINER <i>W. H. H. H.</i>	
DATE CONSIDERED 3-6-02	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

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APPLICANT Jesse Pedigo		FILING DATE December 20, 2001	
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### U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
KS	4,945,313	07/31/90	Synchronous Demodulator Having Automatically Tuned Band-Pass Filter	329	349	06/05/89
	5,117,069	05/26/92	Circuit Board Fabrication	174	261	09/28/90
	5,133,120	07/28/92	Method of Filling Conductive Material into Through Holes of Printed Wiring Boards	29	852	03/15/91
	5,277,854	01/11/94	Methods and Apparatus for Making Grids from Fibers	264	86	06/06/91
	5,332,439	07/26/94	Screen Printing Apparatus for Filling Though-Holes in Circuit Board With Paste	118	213	08/18/92
	5,707,575	01/13/98	Method for Filling Vias in Ceramic Substrates with Composite Metallic Paste	264	104	07/28/94
	5,753,976	05/19/98	Multi-Layer Circuit Having a Via Matrix Interlayer Connection	257	774	06/14/96
	6,015,520	01/18/00	Method for Filling Holes in Printed Wiring Boards	264	104	05/15/97
	6,149,857	11/21/00	Method of Making Films and Coatings Having Anisotropic Conductive Pathways Therein	264	429	12/22/98
	6,184,133	02/06/01	Method of Forming an Assembly Board With Insulator Filled Through Holes	438	667	02/18/00
KS	6,261,501	07/17/01	Resin Sealing Method for a Semiconductor Device	264	272.15	01/22/99

### FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
KS	WO 00/13474	3/9/00	Bryan	-	-		

### OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

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3-6-03

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